International Journal of Applied Electromagnetics and Communication Systems
Volume 1, Issue 02, 2025

Multicarrier PWM Control for Asymmetric Cascaded Multilevel Inverter Modeling and Simulation with Reduced Switches

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Research Article

Date of Submission: 20-01-2025 **Date of Acceptance: 26-03-2025** **Date of Publication: 23-04-2025**

ABSTRACT
In this work, multicarrier pulse width modulation (MC-PWM) control methods are used to model and simulate an asymmetric cascaded multilevel inverter with fewer switches. The paper's ultimate goal is to generate many output levels using the fewest possible semiconductor chips. This article generates a 21-level output voltage using only 11 switches, 3 diodes, and 4 asymmetrical sources. The commutation of the switches is largely dependent on the modulation approach. Due to their lower total harmonic distortion (THD), lower switch ratings, lesser electromagnetic interference, and greater DC link voltages utilized for high-voltage and high-power applications, multilevel inverters perform much better than traditional two-level inverters. In order to enhance multilevel inverter performance and significantly lower overall cost and circuit complexity, a new twenty-one-level reduced switch cascaded multilevel inverter based on a multilevel DC link inverter architecture with reduced switching components is suggested in this study. Simulation is used to demonstrate the efficacy of the suggested system. MATLAB/Simulink is used to run the simulation. The simulation results demonstrate that the suggested multilevel inverter functions correctly to produce the multilayer output waveform with the fewest semiconductor devices and to achieve good dynamic performance with reduced THD.

KEYWORDS: Pulse width modulation (PWM), multicarrier pulse width modulation (MC-PWM), cascaded multilevel inverter (CMLI), multilevel inverter (MLI), and total harmonic distortion (THD).

INTRODUCTION

Nowadays, the need for energy is shifting toward producing electricity using renewable energy sources that can be spread out across a large region. The majority of these sources are renewable since they offer more benefits because they are ecologically benign. Since photovoltaic (PV) energy is seen as a practically infinite and readily available energy resource with an emphasis on greener sources of electricity, especially for remote places where utility power is unavailable, it has increased attention in a broad variety of electrical power applications [1-4]. Everyone in the cosmos can consume solar energy, hence more research into electricity production is not necessary [5–7]. Research on multilayer inverters follows from this.Three kinds of multilevel inverters are distinguished: (i) diode clamped multilevel inverters; (ii) flying capacitor multilevel inverters; and (iii) cascaded H bridge multilevel inverters. The cascaded H bridge multilevel inverter topologies outperform the others. A novel inverter construction with fewer semiconductor devices and more multilayer at the output waveform is being proposed as research continues [8–9]. the investigation of multisampled multilevel inverters and associated control methods to enhance multilevel inverter performance. The various control strategies to be used in multilevel inverters to lower the total harmonic distortion (THD) are also covered. However, they don't

focus on the multilayer inverters' structure [10–11].a method for producing voltage levels of equal breadth by balancing the capacitor voltage. THD is thus decreased. The inverter's structure remains unchanged. They just used the method with a traditional structure, but their THD was higher [12–13]. The switching signals are generated using a novel method. Here, a novel optimization approach is used to generate the modulation signals; it outperforms the previous methods, but the structure of The cascaded multilayer inverter doesn't change. As a result, the number of switches utilized is the same as in the traditional one, but the switching loss is higher. Finding a novel structural method for creating multilayer with smaller semiconductor devices is thus essential [14].

The multilevel inverter fed multiphase induction motor, which uses a diode clamped inverter to provide several levels at the output and drive the five phase motor, and the cascaded H bridge architecture to lower THD. This is used for the performance analysis. Because they use a diode clamped multilevel inverter, there are a lot of semiconductor components, which results in significant losses. The system's performance may be enhanced by adding more layers and replacing it with a new structure [15–16]. The multilevel inverter's closed loop control technique is described, and the control circuit is large, which further raises circuit complexity and decreases the system's efficacy [17–19].

Draw the conclusion that the multilevel inverter's control circuitry. However, the inverter's structure doesn't change. The system's efficiency decreases as the levels increase because the structure is larger and more intricate. This novel structural multilevel inverter uses the fewest possible power semiconductor elements to generate many levels at the output voltage. Additionally, the multi-carrier level shifting PWM has been put into practice. Because there are fewer devices with low switching noise, the THD is significantly decreased.

II. PROPOSED CASCADED MULTILEVEL INVERTER TOPOLOGY

The suggested multilayer inverter connects switches, diodes, and voltage sources in a ladder fashion. Use asymmetrical voltage sources in this architecture, which may be derived from batteries or renewable energy sources like solar, biomass, etc. The asymmetric dc voltage sources are increasing in nature in the order of n, 2n, 3n, 4n, and so on, where n is the lowest DC voltage source magnitude. Figure 1 depicts the main and auxiliary inverter components of the proposed multilayer inverter. In this case, the switching device is the IGBT. In order to get numerous levels at the outputs, anti-parallel diodes are used for the reverse current route. There are less power semiconductor devices used in the suggested system.

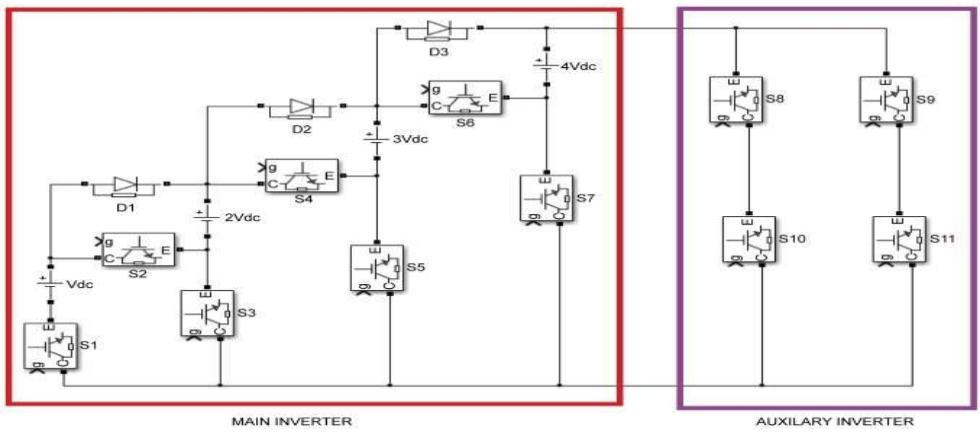


Fig. 1 Structure of proposed multilevel inverter

The switching sequence applied to the suggested architecture to produce a 21-level voltage output is shown in Table 1. Table 1 provides an explanation of how the suggested asymmetric multilevel inverter works. The switch operates in two states: ON and OFF. When the switch is turned on, it is in the saturation area and begins to conduct; when it is turned off, it is in the cut-off region and does not conduct. It can generate 11 voltage levels between 0 and 10Vdc using its 11 operating modes. The following formulas are used to determine the relationship between the number of output levels and the number of semiconductor devices. Let "NDC" represent the number of DC sources or stages. Equation (1) may be used to get the corresponding number of output voltage levels.

$$M=N_{DC}(N_{DC}+1)+1 \quad (1)$$

The number of switches used in this topology is given by the equation (2),

$$NS=2(N_{DC})-1 \quad (2)$$

The number of bypassed diodes used in this topology is given by the equation (3),

$$N_{diodes}=N_{DC}-1 \quad (3)$$

Thus, it can produce 21 voltage levels at the output if four dc sources, three diodes, and seven semiconductor power switches are used. The main inverter and auxiliary inverter are the two components of the suggested system. Table 1 makes it evident that, in comparison to the traditional inverter, the suggested multilayer inverter requires the fewest possible semiconductor devices. The system's efficacy rises as a result of the significant reduction of switching devices and switching losses.

Table 1. Comparison of cascaded H-bridge and proposed inverter

Items	Cascaded H-bridge for 21 output levels	Proposed inverter for 21 output levels
	Single phase	Single phase
Switches	40	11
Diodes	-	3
DC sources	10	4

III. DIFFERENT MODES OF OPERATION

Mode-1: In mode the switch S_1 alone conducts. The current flows through S_1, the source V_1, the diode D_1, D_2 and D_3 to produce the voltage of $1V_{dc}$.

Mode-2: In mode the switch S_3 alone conducts. The current flows through S_3, the source V_2, the diode D_2 and D_3 to produce the voltage of $2V_{dc}$.

Mode-3: In mode the switch S_5 alone conducts. The current flows through S_5, the source V_3, the diode D_3 to produce the voltage of $3V_{dc}$.

Mode-4: In mode the switch S_7 alone conducts. The current flows through S_7 and the source V_4 to produce the voltage of $4V_{dc}$.

Mode-5: In mode the switch S_1 and S_6 conducts. The current flows through S_1, the source V_{dc}, the diode D_1 and D_2, the switch S_6 and the voltage source $4V_{dc}$. Hence it produce the voltage level of $5V_{dc}$ ($V_{dc} + 4V_{dc} = 5V_{dc}$) at the output.

Mode-6: In mode the switch S_3 and S_6 conducts. The current flows through S_3, the source $2V_{dc}$, the diode D_2, the switch S_6 and the voltage source $4V_{dc}$. Hence it produce the voltage level of $6V_{dc}$ ($2V_{dc} + 4V_{dc} = 6V_{dc}$) at the output.
Mode-7: In mode the switch S_5 and S_6 conducts. The current flows through S_5, the source $3V_{dc}$, the switch S_6 and the voltage source $4V_{dc}$. Hence it produce the voltage level of $7V_{dc}$ ($3V_{dc} + 4V_{dc} = 7V_{dc}$) at the output.

Mode-8: In mode the switch S_1, S_4 and S_6 conducts. The current flows through S_1, the source $1V_{dc}$, the diode D_1, the switch S_4, the voltage source $3V_{dc}$, the switch S_6 and the voltage source $4V_{dc}$. Hence it produce the voltage level of $8V_{dc}$ ($1V_{dc} + 3V_{dc} + 4V_{dc} = 8V_{dc}$) at the output.

Mode-9: In mode the switch S_3, S_4 and S_6 conducts. The current flows through S_3, the source $2V_{dc}$, the switch S_4, the voltage source $3V_{dc}$, the switch S_6 and the voltage source $4V_{dc}$. Hence it produce the voltage level of $9V_{dc}$ ($2V_{dc} + 3V_{dc} + 4V_{dc} = 9V_{dc}$) at the output.

Mode-10: In mode the switch S_1, S_2, S_4 and S_6 conducts. The current flows through S_1, the source $1V_{dc}$, the switch S_2, the voltage source $2V_{dc}$, the switch S_4, the voltage source $3V_{dc}$, the switch S_6 and the voltage source $4V_{dc}$. Hence it produce the voltage level of $10V_{dc}$ ($1V_{dc} + 2V_{dc} + 3V_{dc} + 4V_{dc} = 10V_{dc}$) at the output.

Mode-11: In this mode all the switches are in off state. Therefore the output voltage is zero.

The primary inverter can only produce positive and zero voltage levels, as shown in Fig. 1. When every switch is turned off, the output voltage level is zero. Appropriate flipping between the switches yields the other voltage levels. Table 2 shows the switching. The primary inverter's output voltage is always positive and zero. Every half cycle, the voltage polarity must be changed in order for the device to function as an inverter. The H-Bridge inverter circuit, also known as the auxiliary inverter, receives the output of the main inverter for this purpose. Positive voltages from the main inverter are transformed into positive and negative outputs by the auxiliary inverter. The output voltage is produced by the switches S8 and S10, while the negative output voltages are produced by the switches S9 and S11. Zero voltage is produced when S8 through S11 are turned off. To provide numerous output voltage levels, the primary inverter switches S1 through S7 experience high switching frequency. Fundamental switching frequency is used by the auxiliary inverter to transition from S8 to S11.

Table 2. Switching States of 21-level inverter

Modes	Switching States							Output voltage level
	S1	S2	S3	S4	S5	S6	S7	
Mode 1	1	0	0	0	0	0	0	1Vdc
Mode 2	0	0	1	0	0	0	0	2Vdc
Mode 3	0	0	0	0	1	0	0	3Vdc
Mode 4	0	0	0	0	0	0	1	4Vdc
Mode 5	1	0	0	0	0	1	0	5Vdc
Mode 6	0	0	1	0	0	1	0	6Vdc
Mode 7	0	0	0	0	1	1	0	7Vdc
Mode 8	0	0	0	1	0	1	0	8Vdc
Mode 9	0	0	1	1	0	1	0	9Vdc
Mode 10	1	1	0	1	0	1	0	10Vdc
Mode 11	0	0	0	0	0	0	0	0

IV. MODULATION TECHNIQUES

The process of creating the pulses needed to run semiconductor devices in both ON and OFF states is known as

modulation. The switch begins to conduct when the device is in the ON state because it is in the saturation area, and it ceases conducting when it is in the OFF state because it is in the cut-off region. It is crucial to focus on the modulation method since the pulse width determines the output voltage's breadth and level. The
To create the switching pulse, the PWM approach analyzes the carrier and reference waveforms. While the switching frequency of the semiconductor device is determined by the carrier frequency, the reference will be in line frequency.

A. MULTICARRIER PULSE WIDTH MODULATION SCHEMES

The multilevel inverter primarily produces switching signals using the multicarrier PWM approach, and the output waveform resembles a sinusoidal one. The switching signals for the N-level inverter are generated by the multicarrier PWM using (N-1) carriers and the sine wave. It generates the inverter's switching signals by comparing the carrier with the sinusoidal waveform. Phase shifting PWM (PS-PWM) and level shifting PWM (LS-PWM) are the two kinds of carrier waveforms that are distinguished based on their physical structure. The carriers in PS-PWM methods have the same frequency and amplitude but vary in phase from one another. The carriers in LS-PWM methods have the same frequency, phase, and amplitude (peak to peak amplitude), but their biasing levels vary.

B. MULTICARRIER LEVEL SHIFTING PWM TECHNIQUE

For level-shifted multicarrier modulation, there are three alternative PWM strategies with different phase relationships: (i) Phase disposition (PD), in which all carrier waveforms are in phase; (ii) Phase opposition disposition (POD), in which all carrier waveforms above zero reference are in phase and carrier waveforms below zero reference are 180 degrees out of phase; and (iii) Alternate phase disposition (APOD), in which all carrier waveforms above and below zero reference are 180 degrees out of phase with their neighboring carrier.

C. PHASE DISPOSITION LEVEL SHIFTING PWM

The phase disposition PWM technique is implemented carrier-based. To provide switching signals for the circuit, the triangular carriers are typically compared with the sinusoidal reference signal. In the carrier-based approach, switching pulses are produced based on which of the modulation and carrier signals is stronger at any given moment, as seen in Fig. 2.

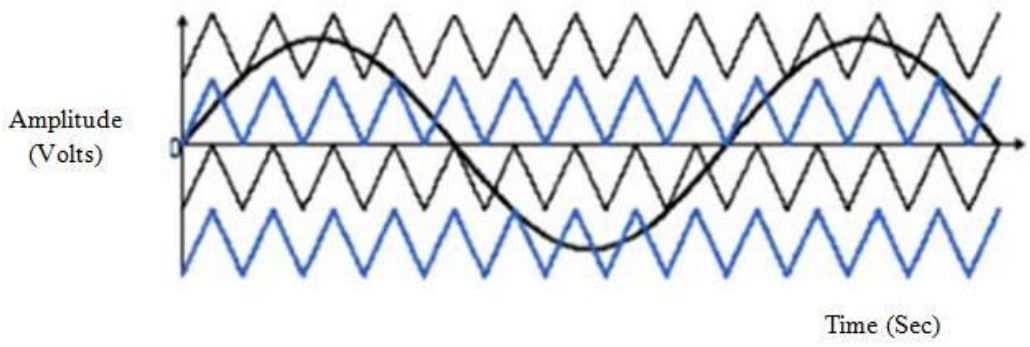


Fig. 2 Multi carrier level shifting phase disposition pulse width modulation (MC-LS-PS-PWM)

The switching signals for an N-level inverter are typically generated by the system using (N − 1) triangular carriers. However, in this case, our suggested method generates N-level output voltages using just (N − 1)/2 carriers. As a result, we have 50% less carrier waveforms in our system in addition to fewer semiconductor devices. As a result, the control system's complexity is decreased, improving the system's overall performance.

SIMULATION RESULTS AND DISCUSSION

The proposed Multilevel Inverter Using MC-PD-LS-PWM architecture generates output voltage waveforms with 21 levels using only 11 switches and diodes with four asymmetrical voltage sources. The main inverter only generates positive voltage levels 1 through 10. Ten positive, ten negative, and one zero level are used by the auxiliary inverter converters to provide a 21-level output at their output voltage.
The 11 switches in the suggested inverter shown in Fig. 1 are designated S1 through S11. The primary inverter, whose output will only be in positive areas, is formed by the switches S1 through S7, three diodes D1, D2, and D3, and four asymmetric voltage sources Vdc, 2Vdc, 3Vdc, and 4Vdc. Eleven voltage levels, ranging from zero to ten volts DC, are produced by it. When switches S8 and S11 are turned on, the auxiliary inverter—a traditional H bridge inverter—produces positive voltage levels ranging from 0 to 10 Vdc. Negative voltage levels between zero and −10Vdc are produced when S9 and S10 are turned on. As a result, the suggested inverter generates 21 voltage levels, ranging from +10Vdc to −10Vdc. In this case, 25 volts of Vdc are employed. As a result, it may produce an amplitude between +250 and -250 volts.

Figure 3 displays the output voltage waveform with 21 voltage levels. It shows the proposed asymmetric cascaded multilevel inverter's single phase output voltage. Although the inverter's real output is between +250 and -250 volts, various losses cause the output to be between +240 and -240 volts. The multicarrier level shifting pulse width modulation signals are seen in Fig. 4.

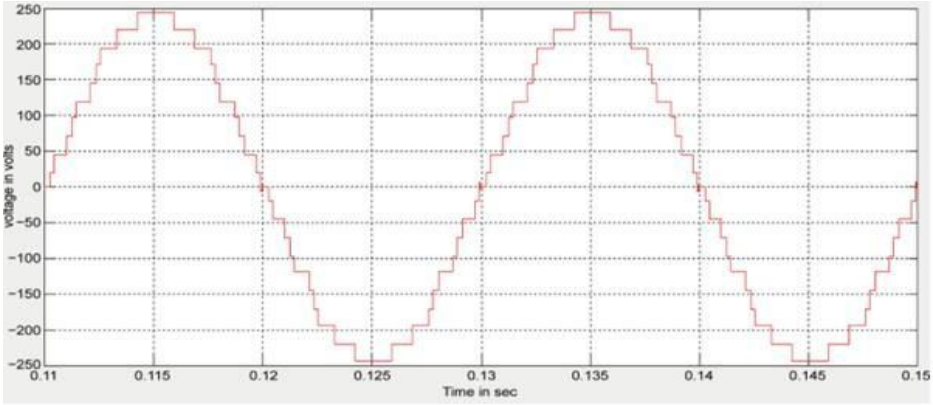


Fig. 3 Single phase 21 level Output line voltage waveform

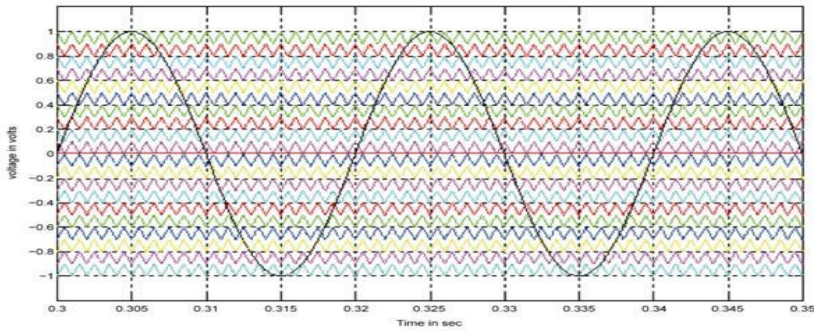


Fig. 4 Output waveform of MC-LS-PS-PWM

The reference signals in this case are sine waves, and the carriers are triangle signals. Since we are using several carriers, this falls under the multicarrier categorization; the carrier signals have the same amplitude and phase but different distribution levels. The overall harmonic distortion in the output voltage of the suggested multilevel inverter using level shifting pulse width modulation is shown in Fig. 5.

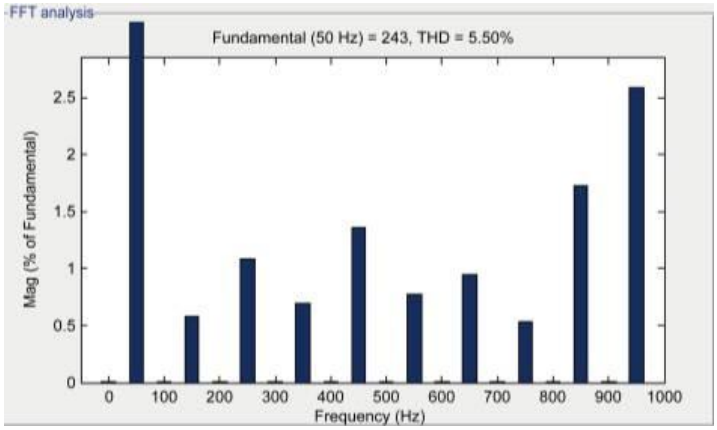


Fig. 5 THD of voltage using MC-LS-PS-PWM

V. CONCLUSION

A platform for multicarrier PWM control approaches is used to describe and simulate an asymmetric cascaded multilevel inverter with fewer switches. MATLAB/Simulink is used to create and simulate the configuration for the suggested system. By lowering the THD, the MC-LS-PD-PWM approach helps to further enhance the inverter's performance. This technology ensures minimal THD, a strong performance, a quick transient response, and a high disturbance rejection capacity. Additionally, the simulation demonstrates that numerous voltage levels may still be produced without shunting down the whole system in the event of a switch failure. The efficacy of the suggested multilayer inverter, which employs less power semiconductor devices, is further shown by the simulation result. The findings unequivocally demonstrate that the suggested design can function as a multilayer inverter with fewer switches and carriers for PWM.

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